a synchronizing circuit for coupling said core of said first processor to said core of said second processor; and

a memory circuit for coupling said local memory of said first processor to said local memory of said second processor.

B1

7. (amended) The apparatus of Claim 6, wherein said second [first] processor is the main processor of said apparatus.

B2

9. (amended) The apparatus of Claim 7, wherein said second [first] processor is a digital signal processor "DSP".

B3

12. (amended) The apparatus of Claim 6, wherein said program [local] memory of said second processor is ROM memory.

B4

18. (amended) The apparatus of Claim 6, wherein said second processor comprises:

an incremental register; and

a program memory connected to the incremental register.[;]

19. (amended) The apparatus of Claim 6, wherein an instruction set is provided to said first [protocol] processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions:

integers corresponding to arithmetic and logic operations on integer numbers;

transfer corresponding to the transfer operations between a register in said protocol processor and memory; and

monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor.

Cancel Claims 20-33 without prejudice.

Please add the following new claims:

34. The apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing.

B5

35. The apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type.?

36. An apparatus, comprising:

a first processor comprising a core, a program memory and a local memory;

a second processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor; and

one and only one common memory coupling said local memory of said first processor to said local memory of said second processor.

37. An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

38. An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being suited to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

a common memory coupling said local memory of said main processor to said local memory of said protocol processor.

B5

39. An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being suited to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

REMARKS

Applicants submit a separate letter proposing the labeling of the boxes in Figures 1, 2, 5, 7, 8, 13, 17 and 17, as requested by the Examiner. Applicants respectfully request approval.

Claims 12, 18 and 19 have been amended better to define the invention and overcome the 35 U.S.C. 112 rejections.

Claims 6-25 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (5,237,686). Applicants respectfully traverse.

Independent Claim 6, as amended, requires and positively recites, "a first **processor for performing scalar processing**, said first processor comprising a core, a program memory and a local memory", "a second processor **for performing vector processing**, said second processor comprising a core, a program memory and a local memory", "a synchronizing circuit for coupling